THE INVENTION CLAIMED IS:

1. A method for manufacturing an integrated circuit structure, comprising:

providing a semiconductor substrate;

forming at least one oxide-nitride-oxide dielectric layer above the semiconductor substrate; and

forming at least one implantation into at least one area of the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer subsequent to the formation of the oxide-nitride-oxide dielectric layer.

2. The method of claim 1 wherein the implantation is a channel implantation.

3. The method of claim 1 wherein the implantation is a well and threshold implantation.

4. The method of claim 3 wherein the well and threshold implantation is into one of an array area and a periphery area over the semiconductor substrate, and further comprising forming another well and threshold implantation into the other of the array and periphery areas over the semiconductor substrate.

5. The method of claim 4 further comprising forming a channel implantation into the array area and the periphery area.

6. A method for manufacturing an integrated circuit structure, comprising:

providing a semiconductor substrate;

forming an oxide-nitride-oxide dielectric layer on the semiconductor substrate;

forming a layer of polysilicon on the oxide-nitride-oxide dielectric layer;

forming a nitride hardmask layer on the layer of polysilicon;

patterning and forming a composite mask on the nitride hardmask;

etching the nitride hardmask, layer of polysilicon, oxide-nitride-oxide dielectric layer, and semiconductor substrate to form shallow trench isolation trenches;

filling the shallow trench isolation trenches with an oxide gap fill;

polishing the oxide gap fill;

removing the nitride hardmask;

covering a periphery area over the semiconductor substrate with a photoresist mask; and

performing well and threshold implantation over an array area above the semiconductor substrate into the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer.

7. The method of claim 6 further comprising, prior to the step of covering the periphery area over the semiconductor substrate with a photoresist mask:

covering the array area over the semiconductor substrate with a photoresist mask;

removing the polysilicon and the oxide-nitride-oxide dielectric in the periphery area; and

performing well and threshold implantation over the periphery area into the semiconductor substrate.

8. The method of claim 7 further comprising forming a channel implantation over the array area and the periphery area into the semiconductor substrate therebeneath.

9. The method of claim 8 further comprising:

forming a gate dielectric layer over at least portions of the periphery area;

forming at least one control gate layer over at least portions of the gate dielectric layer; and

forming an interlayer dielectric layer over at least portions of the array area and the periphery area.

10. The method of claim 9 further comprising forming at least one electrical contact through the interlayer dielectric layer to at least one portion of the control gate layer therebeneath, and at least one electrical contact through the interlayer dielectric layer to at least one portion of the polysilicon therebeneath.

11. An integrated circuit structure, comprising:

a semiconductor substrate;

at least one oxide-nitride-oxide dielectric layer above the semiconductor substrate; and

at least one implantation region in at least one area of the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer having diffusion unaffected by the oxide-nitride-oxide dielectric layer.

12. The integrated circuit structure of claim 11 wherein the implantation is a channel implantation.

13. The integrated circuit structure of claim 11 wherein the implantation is a well and threshold implantation.

14. The integrated circuit structure of claim 13 wherein the well and threshold implantation is into one of an array area and a periphery area over the semiconductor substrate, and further comprising another well and threshold implantation into the other of the array and periphery areas over the semiconductor substrate.

15. The integrated circuit structure of claim 14 further comprising a channel implantation formed into the array area and the periphery area.

16. An integrated circuit structure, comprising:

a semiconductor substrate having an array area and a periphery area;

an oxide-nitride-oxide dielectric layer formed on the array area on the semiconductor substrate;

a layer of polysilicon formed on the oxide-nitride-oxide dielectric layer;

the layer of polysilicon, oxide-nitride-oxide dielectric layer, and semiconductor substrate being etched to form shallow trench isolation trenches;

a polished oxide gap fill filling the shallow trench isolation trenches; and

a well and threshold implantation region in the semiconductor substrate beneath the oxide-nitride-oxide dielectric layer over the array area, the well and threshold implantation having diffusion unaffected by the oxide-nitride-oxide dielectric layer.

17. The integrated circuit structure of claim 16 further comprising a well and threshold implantation into the semiconductor substrate in the periphery area.

18. The integrated circuit structure of claim 17 further comprising a channel implantation over the array area and the periphery area into the semiconductor substrate therebeneath.

19. The integrated circuit structure of claim 18 further comprising:

a gate dielectric layer over at least portions of the periphery area;

at least one control gate layer over at least portions of the gate dielectric layer; and

an interlayer dielectric layer over at least portions of the array area and the periphery area.

20. The integrated circuit structure of claim 19 further comprising at least one electrical contact through the interlayer dielectric layer to at least one portion of the control gate layer therebeneath, and at least one electrical contact through the interlayer dielectric layer to at least one portion of the polysilicon therebeneath.